

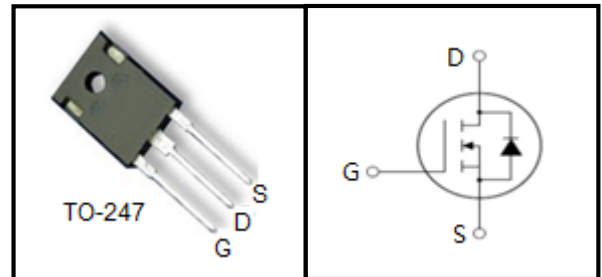
650V Super-Junction Power MOSFET

FEATURES

- $BV_{DSS}=650\text{ V}$, $I_D=55\text{ A}$
- $R_{DS(on)}:65\text{ m}\Omega$ (Max) @ $V_{GS}=10\text{ V}$
- Very low FOM $R_{DS(on)} \times Q_g$
- 100% avalanche tested
- RoHS compliant

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



Device Marking and Package Information

Device	Package	Marking
MPSW65M065	TO-247	MP65M065

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DSS}	650	V
Continuous Drain Current	I_D	55	A
Pulsed Drain Current (note1)	I_{DM}	165	A
Gate-Source Voltage	V_{GSS}	± 30	V
Single Pulse Avalanche Energy (note2)	E_{AS}	1200	mJ
MOSFET dv/dt ruggedness, $V_{DS}=0\dots 400\text{ V}$	dv/dt	50	V/ns
Reverse diode dv/dt, $V_{DS}=0\dots 400\text{ V}$, $I_{SD} \leq I_D$	dv/dt	15	V/ns
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	391	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max.	R_{thJC}	0.32	K/W
Thermal Resistance, Junction-to-Ambient, Max.	R_{thJA}	62	



Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	--	--	100	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 0.25mA$	2.5	--	4.5	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 26.5A$	--	0.052	0.065	Ω
Gate Resistance	R_G	$f = 1.0MHz, \text{open drain}$	--	2.0	--	Ω
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 50V, f = 1.0MHz$	--	4747	--	μF
Output Capacitance	C_{oss}		--	290	--	
Reverse Transfer Capacitance	C_{rss}		--	30	--	
Effective output capacitance, energy related	$C_{o(er)}$	$V_{GS}=0V, V_{DS}=0...400V$	--	161	--	
Effective output capacitance, time related	$C_{o(tr)}$	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$	--	817	--	
Total Gate Charge	Q_g	$V_{DD} = 400V, I_D = 25A, V_{GS} = 10V$	--	115	--	nC
Gate-Source Charge	Q_{gs}		--	23	--	
Gate-Drain Charge	Q_{gd}		--	40	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 25A, V_{GS} = 10V, R_G = 1.9\Omega$	--	22	--	ns
Turn-on Rise Time	t_r		--	10	--	
Turn-off Delay Time	$t_{d(off)}$		--	120	--	
Turn-off Fall Time	t_f		--	8	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	55	A
Pulsed Diode Forward Current	I_{SM}		--	--	165	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 55A, V_{GS} = 0V$	--	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R = 400V, I_F = 30A, di_F/dt = 100A/\mu s$	--	600	--	ns
Reverse Recovery Charge	Q_{rr}		--	13.0	--	μC
Peak Reverse Recovery Current	I_{rrm}		--	46.0	--	A

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 10mH, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width $\leq 300\mu s, \text{Duty Cycle } \leq 1\%$



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

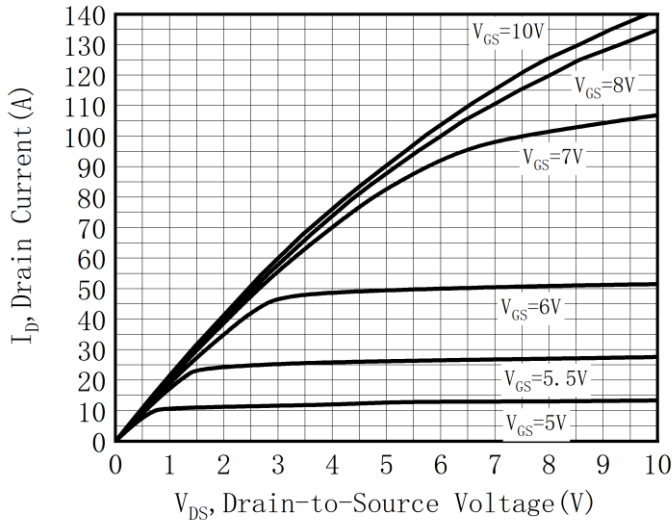


Figure 2. Transfer Characteristics

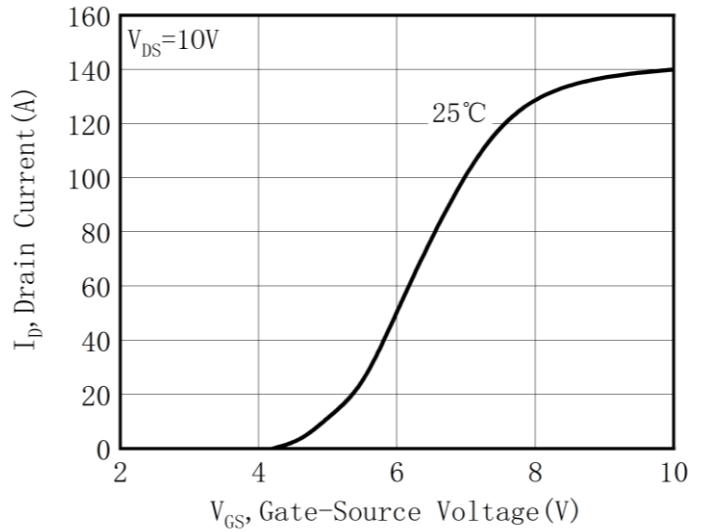


Figure 3. On-Resistance vs Drain Current

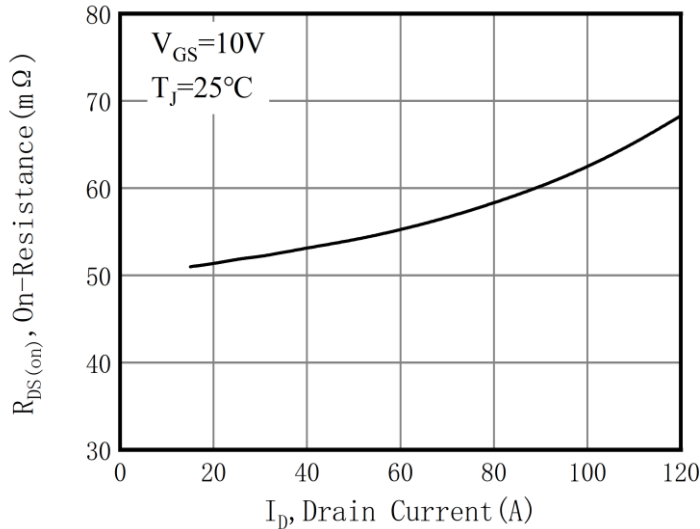


Figure 4. Capacitance

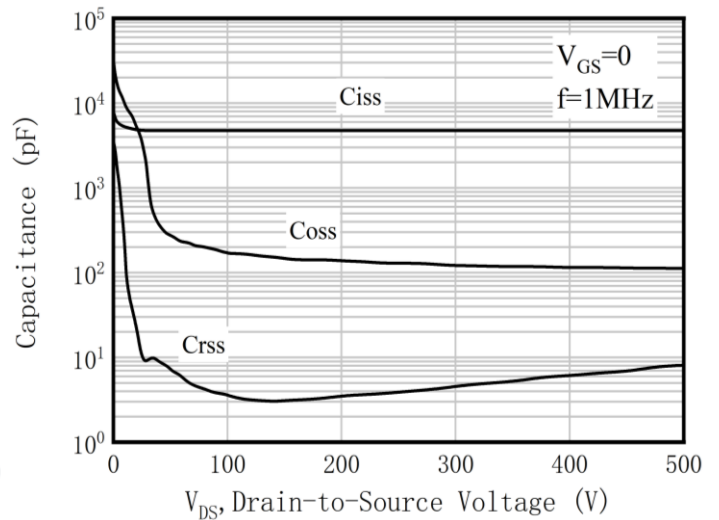


Figure 5. Gate Charge

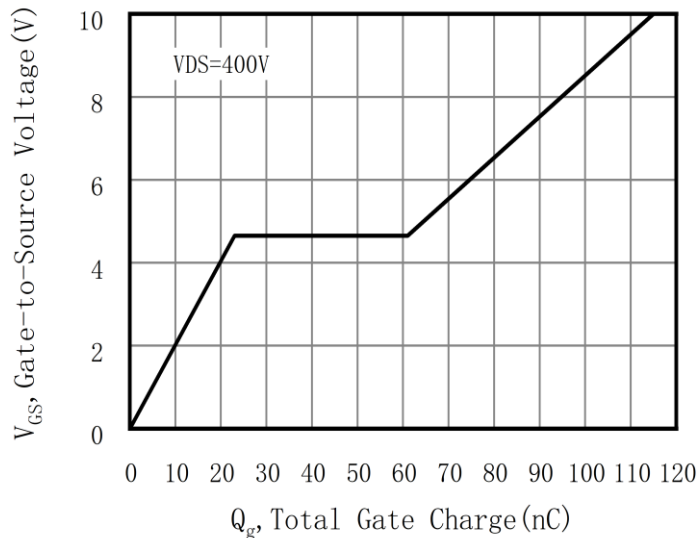
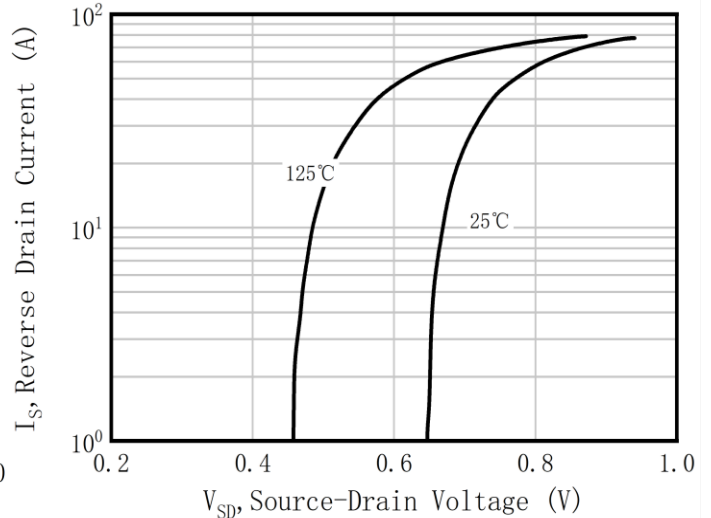


Figure 6. Body Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. On-Resistance vs Junction Temperature

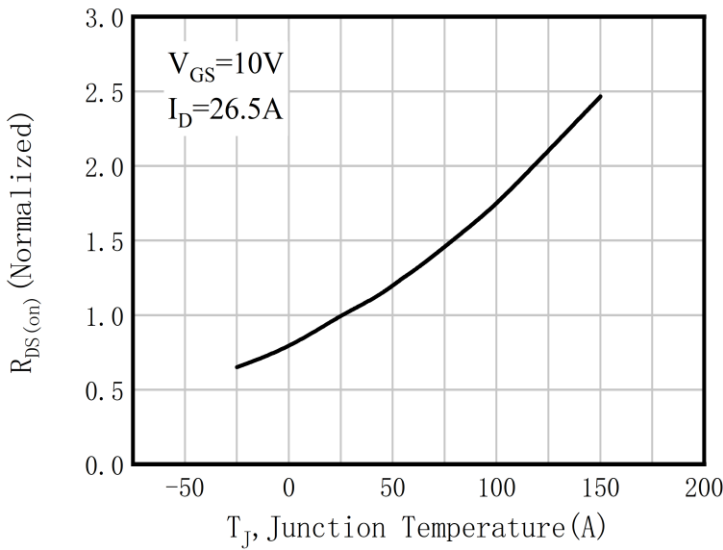


Figure 8. Threshold Voltage vs Junction Temperature

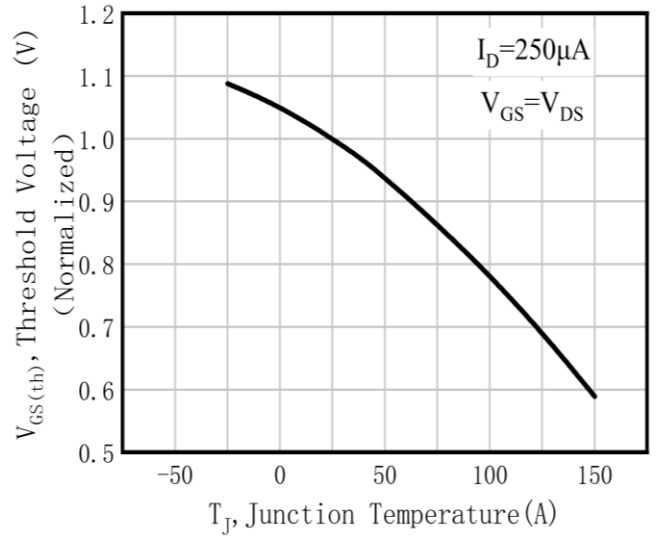


Figure 9. Transient thermal Impedance

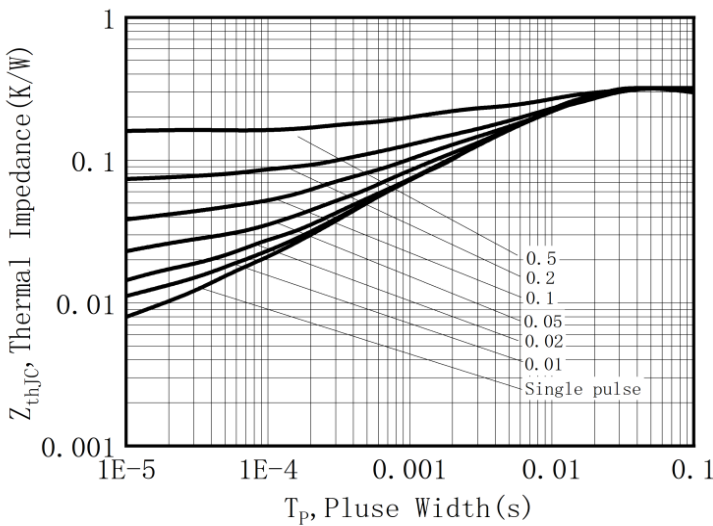


Figure 10. Safe Operating Area

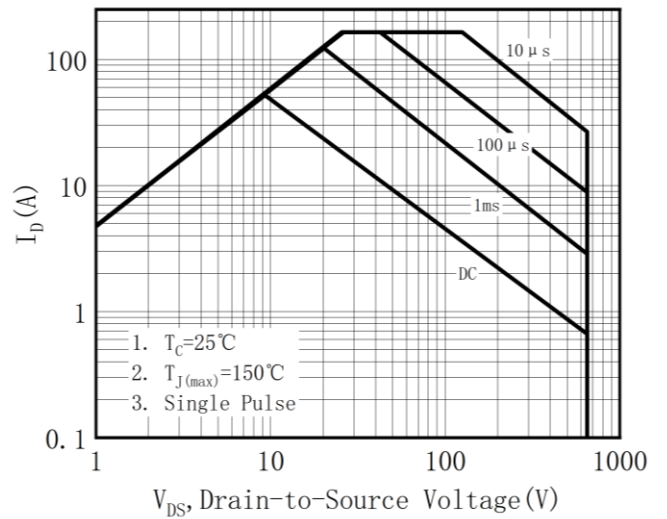


Figure 11. C_{oss} stored energy

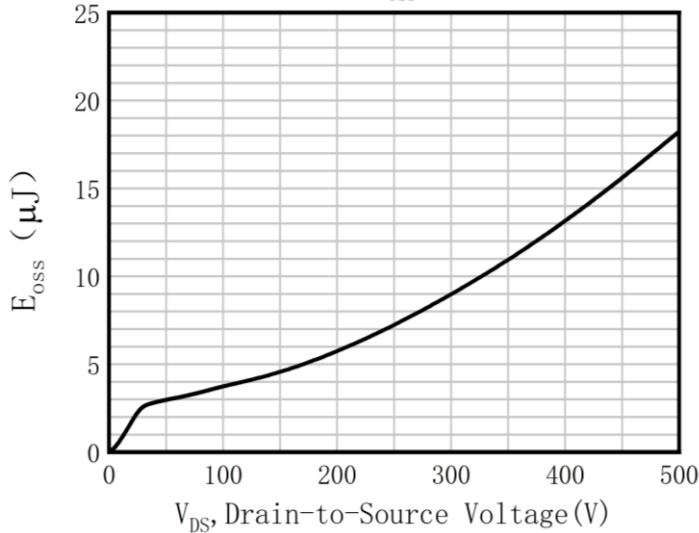


Figure A: Gate Charge Test Circuit and Waveform

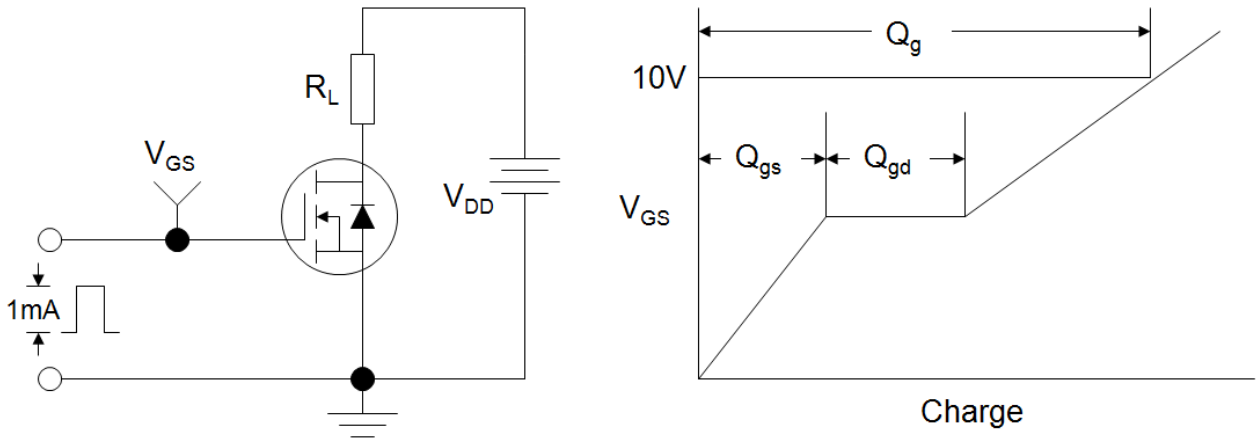


Figure B: Resistive Switching Test Circuit and Waveform

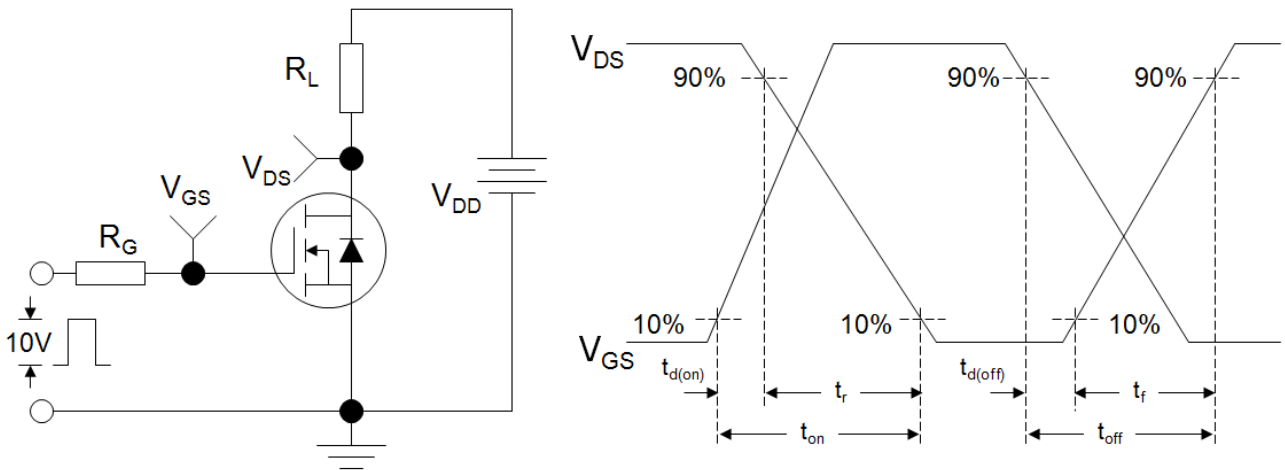
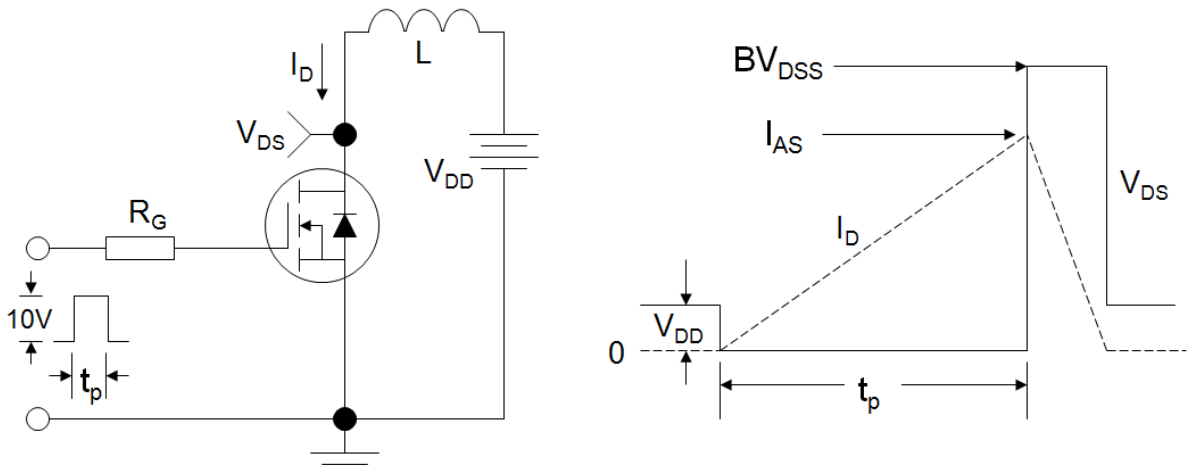
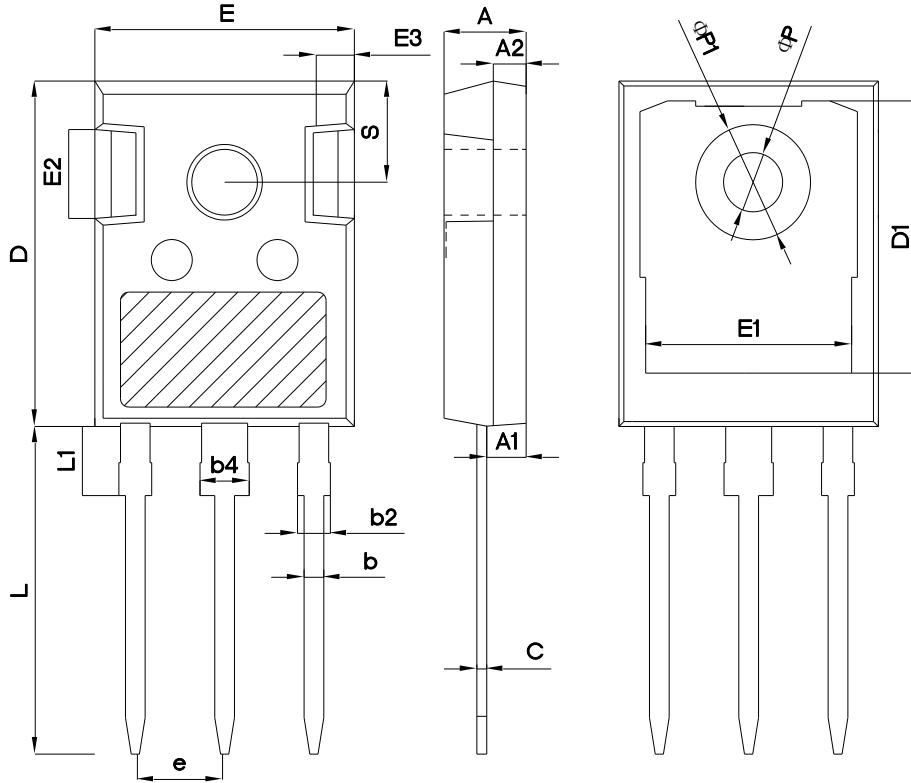


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



TO-247



SYMBOL	mm		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b2	1.91	2.01	2.21
b4	2.91	3.01	3.21
c	0.51	0.61	0.75
D	20.80	21.00	21.30
D1	16.25	16.55	16.85
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.80	5.00	5.20
E3	2.30	2.50	2.70
e	5.44BSC		
L	19.82	19.92	20.22
L1	-	-	4.30
ΦP	3.40	3.60	3.80
ΦP1	-	-	7.30
S	6.15BSC		



Revision: 2022-10-10, Ver 1.0

Revision	Date	Subjects (major changes since last revision)
1.0	2022-10-10	Initial version